Application Note

Anritsu

Active Optical Cable (AOC) Evaluation Method

InfiniBand™ 56G-IB-FDR (14 Gbit/s x4)
QSFP+ Cable Compliance Test

MP1800A Series
Signal Quality Analyzer

Index

1. Introduction 2
2. High-speed Electric Interface Specifications 3
3. Method of Implementation 9
4. Conclusion 24
Appendix 24
References 24

1. Introduction

Computers have seen huge increases in processing power as semiconductor process technologies become finer and CPUs become multicore. Supercomputers have become 100,000 times faster in the last 20 years, but on the other hand data volumes have ballooned and communications processing using parallel-processing configurations have reached a bottleneck. High-efficiency communications methods are needed in future instead of the previously used Gigabit Ethernet.
InfiniBand™ is one interconnect standard used in High Performance Computing (HPC) fields such as supercomputers. At November 2012, 45% of all HPC used by Top500 companies (www.top500.org) were reported as using the InfiniBand standard. Due to its low latency and low cost, there is increasing interest in using InfiniBand for connecting data center servers. Like Fibre Channel, PCIe and Serial ATA, InfiniBand communications technology uses duplex serial transfers and a wide bandwidth is achieved by binding multiple channels together.
Today, the Active Optical Cable (AOC), especially parallel multi-lane cables using QSFP+ modules, is one of the most important devices used by high-speed interconnects, such as InfiniBand, and accurate cable testing is necessary to ensure reliable data transmissions and interoperability.
This document explains how to evaluate the QSFP+ type AOC for 56G-IB-FDR, which consists of four 14-Gbps parallel lanes. Section2 outlines the specification of the high speed electrical interface. Section 3 outlines how to perform the measurement procedure using actual measuring instruments, such as the Anritsu MP1800A Signal Quality Analyzer.

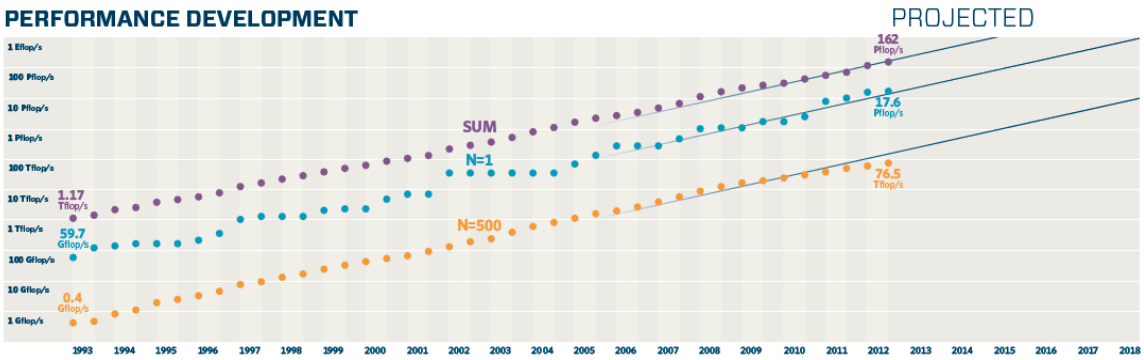


Fig. 1-1 Supercomputer Processing Performance, Source: Top 500

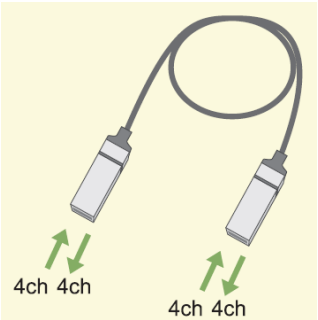


Fig. 1-2 QSFP+ Active Optical Cable (AOC)

2. High-speed Electric Interface Specifications

The InfiniBand Trade Association (IBTA) proposing the InfiniBand standard classifies it by serial transfer speeds as follows: SDR (Single Data Rate, 2.5G), DDR (Double Data Rate, 5G), QDR (Quad Data Rate, 10G), FDR (Fast Data Rate, 14G), EDR (Enhanced Data Rate, 26G). Moreover, each data rate is standardized for four and twelve channel parallel transfers. The InfiniBand Architecture Specification Volume 2 Release 1.3[1] (hereafter InfiniBand AS V2R1.3) standard released in November 2012 formally settled on the 56G-IB-FDR standard using four-channel parallel transfer FDR (14G).

Table 2-1 InfiniBand Link Data Rates
(Table 39 in InfiniBand AS V2R1.3 Vol 2 Chapter 6)

InfiniBand rate designator	Per-lane signaling rate, GBd	Unit Interval (UI) or bit period, ps	Codec	Aggregate full duplex throughput, GB/s (GBytes/sec) Link Designator			
				4X interface		12X interface	
SDR	2.5	400	8b/10b	(1+1) GB/s	10G-IB-SDR	(3+3) GB/s	30G-IB-SDR
DDR	5.0	200	8b/10b	(2+2) GB/s	20G-IB-DDR	(6+6) GB/s	60G-IB-DDR
QDR	10.0	100	8b/10b	(4+4) GB/s	40G-IB-QDR	(12+12) GB/s	120G-IB-QDR
FDR	14.0625	71.1111	64b/66b	(6.8+6.8) GB/s	56G-IB-FDR	(20.4+20.4) GB/s	168G-IB-FDR
EDR	25.78125	38.7878	64b/66b	(10+10) GB/s	104G-IB-EDR	(30+30) GB/s	312G-IB-EDR

The AOC electrical interface is standardized by InfiniBand AS V2R1.3 Vol 2 Chapter 6 as a high-speed electrical interface of the cable for connecting between two Link End Nodes. The Link End Node is the InfiniBand interface such as the Host Cable Adapter built into a Server, switch or router. Fig. 2-1 shows an outline of the connection. Several types of InfiniBand high-speed electrical interfaces are defined but AOC is a Full Limiting Active Cable; in other words both ends of an AOC cable have a limiting amp and repeater circuit built into the input/output section.

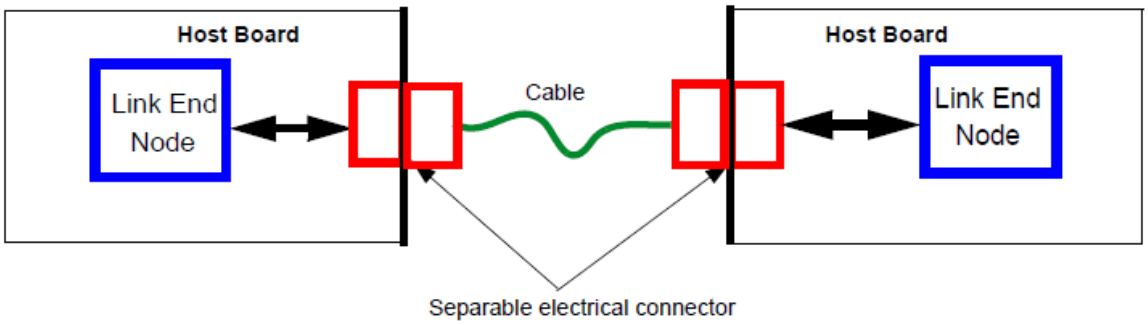


Fig. 2-1 High-level Topology Block Diagram
(Fig. 59 in InfiniBand AS V2R1.3 Vol 2 Chapter 6)

The cable high-speed electrical interface standard can be classified broadly into two parts:

(1) Cable Input Electrical Specifications
(2) Cable Output Electrical Specifications

The cable must meet the output specifications of item (2) when inputting a signal specified in item (1).

The actual cable evaluation is broadly divided into two steps in line with the above standards:

(1) Input Calibration Step: Generation and confirmation of stress signal for input to cable
(2) Output Measurement Step: Input of generated stress signal to cable and quality evaluation of cable signal output

The steps and target specifications are outlined below.

(1) Cable Input Electrical Specifications

The Cable Input Electrical Specifications are listed in Table 2-2. At cable evaluation, calibration is performed by generating a stress signal targeting these specifications.

Table 2-2 FDR Limiting Active Cable Input Electrical Specifications (Table 72 in InfiniBand AS V2R1.3 Vol 2 Chapter 6)

Symbol	Parameter	Specification value(s)	Unit	Conditions
X1, X2	eye mask parameter, time; see Figure 72 on page 240	0.11, 0.31	UI	At TP6a, at FDR and higher data rates Hit ratio=$5x10^{-5}$
Y1, Y2	eye mask parameter, voltage	95, 350	mV	
	Crosstalk signal Vpk-pk	+/- 20% (See Conditions)	mV	At TP6a. Co-propagating aggressors. Crosstalk signal Vpk-pk to match lane under test, to within +/- 20%.
	Crosstalk signal transition time, 20%-80%	24	ps	
	Crosstalk calibration signal Vpk-pk, each aggressor	450	mV	At TP7a. Counter-propagating aggressors. Apply during crosstalk calibration only[a]
	Crosstalk calibration signal transition time, 20%-80%	17	ps	

Symbol	Parameter	Max	Min	Unit	Conditions
	Single-ended input voltage	4	-0.3	V	At TP6a
V_{CM}	AC common mode input voltage tolerance (RMS)	20		mV	At TP6a
DDPWS	Data Dependent Pulse Width Shrinkage	0.11		UI	At TP6a
J2	J2 Jitter tolerance	0.19		UI	At TP6a
J9	J9 Jitter tolerance	0.34		UI	At TP6a
S_{DD11}	Differential input return loss	Eq. 1 on page 251		dB	50 MHz to 14.1 GHz at TP5a
S_{CC11}	Common mode input return loss	-2		dB	200 MHz to 14.1 GHz at TP5a
S_{DC11}	Common mode to differential reflection	Eq. 2 on page 251		dB	50 MHz to 14.1 GHz at TP5a

a. Please refer to CIWG Method of Implementation (MOI) document Active Time Domain Testing for detailed specification of testing methodology and parameters.

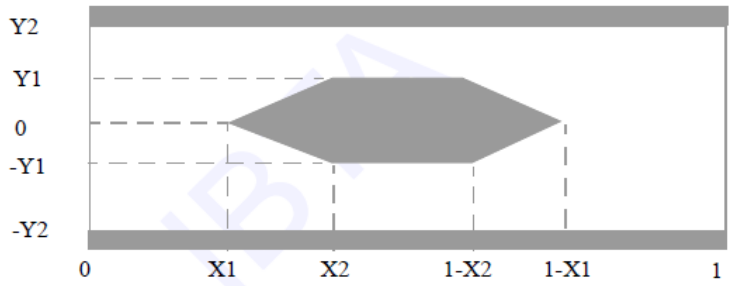


Fig. 2-2 Input Eye Mask (Fig. 72 in InfiniBand AS V2R1.3 Vol 2 Chapter 6)

As shown in Fig. 2-3, stress signal calibration uses a Pulse Pattern Generator (PPG) and oscilloscope. A QSFP interface connector is used to make a direct connection between the Module Compliance Board (MCB) and Host Compliance Board (HCB) and measuring instruments are connected using the SMA connector provided on each board.
The PPG output data amplitude and jitter amount are adjusted to create a waveform satisfying the specified Eye Mask and jitter amount. This test signal is called the Victim signal[3] affected by crosstalk.
Emphasis technology is also required to compensate Data Dependent Pulse Width Shrinkage (DDPWS)[2] of the input signal. The DDPWS must be adjusted in a specified range during calibration. Jitter is added to the victim signal at the cable input until the J2 and J9[2] jitter amplitude becomes the target number. The Eye Amplitude is adjusted so the Eye opening becomes the pre-determined Eye Mask.

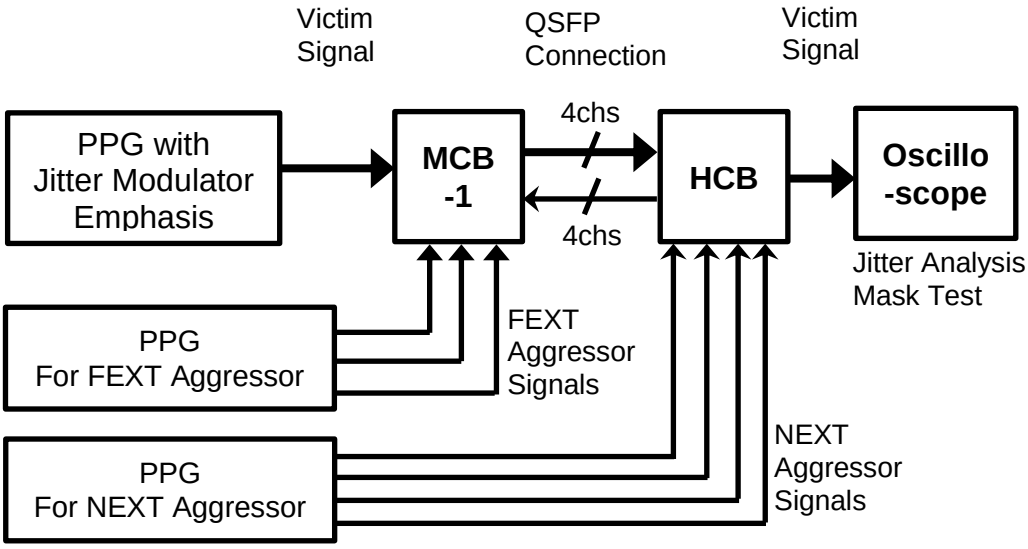


Fig. 2-3 Input Calibration Concept Diagram

The 56G-IB-FDR cable supports four channels in both directions, or transmission of eight signals. Consequently, evaluating Inter-symbol Interference (ISI)[2] and crosstalk effects for a multi-lane cable requires one victim signal and N aggressor signals (N = 7 for QSFP+). The aggressor signals are divided into Far End Crosstalk (FEXT) and Near End Crosstalk (NEXT) components. The rules for each Bitrate, Eye Amplitude, etc., are defined in the Method of Implementation (MOI) produced by The IBTA Compliance and Interoperability Working Group (CIWG).
The oscilloscope must support an analog bandwidth of better than 17 GHz as well as mask test and jitter analysis functions.

(2) Cable Electrical Output Specifications

Table 2-3 lists the Cable Output Electrical specifications. At cable evaluation, the stress waveform generated at the calibration step is input to the DUT QSFP cable and the output waveform is monitored.

Table 2-3 FDR Limiting Active Cable Output Electrical Specifications (Table 73 in InfiniBand AS V2R1.3 Vol 2 Chapter 6)

Symbol	Parameter	Specification value(s)	Unit	Conditions
X	eye mask parameter, time	0.30	UI	Hit ratio=5E-5 with 100 Ohm load at TP7a (Note [a])
Y1, Y2	Diff. unsigned output voltage range 0 (required) range 1 (optional) range 2 (optional)	 50, 225 100, 350 150, 450	mV	
	Crosstalk signal Vpk-pk, each aggressor	700	mV	At TP6a. Counter-propagating aggressors.[b]
	Crosstalk signal transition time, 20%-80%	24	ps	

Symbol	Parameter	Max	Min	Unit	Conditions
Vout	Single-ended output voltage	4.0	-0.3	V	Referred to Signal Ground; measured at TP7a
V_{CM}	AC common mode output voltage (RMS)	20		mV	at TP7a
	Termination mismatch	5		%	1 MHz; at TP7a
S_{DD22}	Differential output return loss	Eq. 1 on page 251		dB	50 MHz to 15 GHz at TP7a
S_{CC22}	Common mode output return loss	-2		dB	200 MHz to 15 GHz at TP7a
S_{DC22}	Common mode to differential reflection	Eq. 2 on page 251		dB	50 MHz to 15 GHz at TP7a
t_r, t_f	Output transition time		17	ps	20-80%
J2	J2 Jitter	0.44		UI	At TP7a
J9	J9 jitter	0.69		UI	At TP7a

a. Output range is set for QSFP+ interfaces using page 03, addresses 238 & 239; see Section 8.5.
For CXP interfaces, output range is set using Rx Addresses 62-67; see Section 8.7.0.2.
b. Please refer to CIWG Method of Implementation (MOI) document Active Time Domain Testing for detailed specification of testing methodology and parameters.

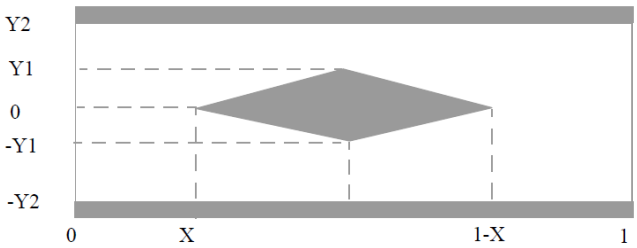


Fig. 2-4 Output Eye Mask (Fig. 72 in InfiniBand AS V2R1.3 Vol 2 Chapter 6)

As shown in Fig. 2-5, the QSFP cable output signal is connected to the oscilloscope via the second MCB. The Eye Mask test is conducted at the cable output by measuring the degraded eye opening determined by at least the minimum tolerable number for the data transmission specified by the standards organization, such as InfiniBand or CEI.

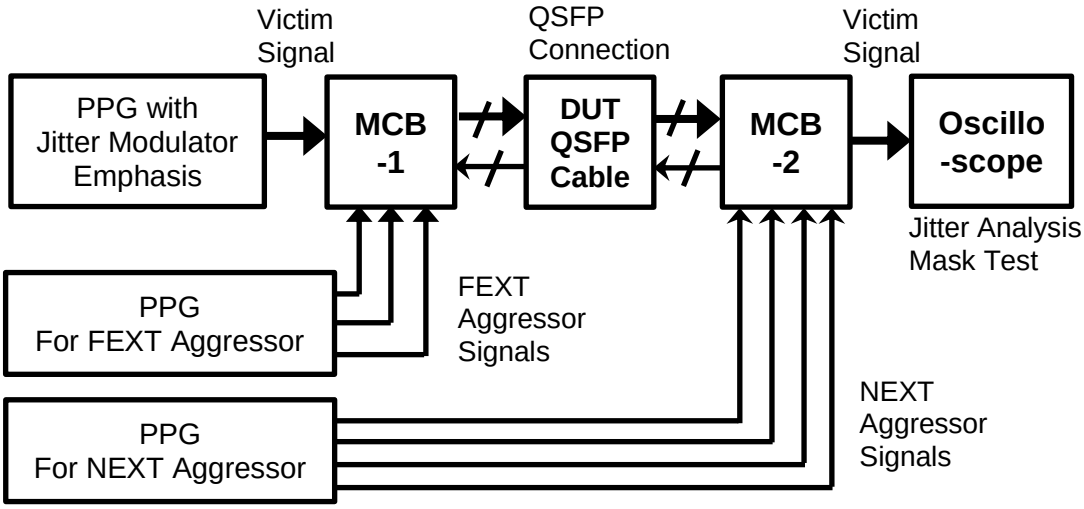


Fig. 2-5 Output Measurement Concept Diagram

3. Method of Implementation

This section explains how to perform the measurement procedure using actual measuring instruments, such as the Anritsu MP1800A Signal Quality Analyzer.

Notice) For latest measurement method of compliance test, refer to the Active Cable Time-Domain Testing MOI provided by IBTA.

3.1 Test Setup and Configuration

The following pieces of test equipment are required for the 56G-IB-FDR AOC test:

(1) BERT for Victim Signal
- 14.1 Gbps Pulse Pattern Generator (PPG)
- 14.1 Gbps Error Detector: Not mandatory
- 14.1 GHz synthesizer: Master Clean Clock
- Jitter Modulator: For adding Random Jitter (RJ) and Deterministic Jitter (DJ). A full-rate clean clock output is required for aggressor signals.

(2) Emphasis Box for Victim Signal
- 14.1 Gbps Emphasis Signal Generator

(3) BERT for Aggressor Signal
- Two 14.1 Gbps PPGs for aggressors: Divided into seven aggressor signal channels by Divider Network and requiring differential 700 mVpp (single-end 350mV) at Divider Network output.
- 14.1 GHz Synthesizer: Master Clean Clock. This clock must not be synchronized with the victim synthesizer.

(4) Oscilloscope for Eye Pattern Analysis
- 14.1 Gbps Oscilloscope: Bandwidth of better than 17 GHz

(5) Accessories
- Two Module Compliance Test Boards[1]
- One Host Compliance Test Board[1]
- Twelve power dividers: To produce seven differential aggressor signals from two PPGs, with K-type connector
- Sixteen phase-matched SMA (or K) cables for aggressor signals

The Anritsu MP1800A Signal Quality Analyzer series is recommended for use as the BERT for the victim and aggressor signals. The recommended configurations are as follows:

Table 3-1 Recommended BERT Configuration for Victim Signal

MP1800A (with Opt-015)			
Slot	Model Name	Model Number	Option number
1	Synthesizer	MU181000A/B	
2			
3	14.1G PPG	MU181020B	002, 005,
4	14.1G ED	MU181040B	002, 005, 030
5	Jitter Modulation Source	MU181500B	
6			

Note: MU181000B has 4 port clock output and is useful for connection.

Table 3-2 Recommended Emphasis Box Configuration for Victim Signal

Model Name	Model Number	Option number
4 Tap Emphasis (14.1G)	MP1825B	001, 005
4 Tap Emphasis (28.1G)		002

Note: Both the 14.1G and 28.1G versions can be used.
Opt-002 (28.1G version) was used at the IBTA Plugfest22.

Table 3-3 Recommended BERT Configuration for Aggressor Signals

MP1800A (with Opt-015)			
Slot	Model Name	Model Number	Option number
1	PPG	MU181020B	002, 005, 013
2	PPG	MU181020B	002, 005, 013
3	Synthesizer	MU181000A/B	
4			
3-6	Not used		

Note: Requires following accessories to double synthesizer clock from 7 GHz to 14 GHz for this aggressor configuration.

- P0047A Frequency Doubler
- Z1340A 13 GHz Band Pass Filter (BPF)

3.2 Test Procedure

As described in section 2, actual cable evaluation is performed in the order of the Input Calibration Step and Output Measurement Step as follows. Note that the connections are different at each step.

Step 1 : Input Calibration

Step 1-1 : Victim and Co-Propagating Crosstalk (FEXT) Calibration

- Co-Propagating Input Aggressors calibration
- Counter-Propagating Output Aggressors calibration
- Victim calibration

Step 1-2 : Counter-Propagating (NEXT) Calibration

- Counter-Propagating Input Aggressors calibration

Step 2 : Output Measurement

Step 1: Input Calibration

Step 1-1: Victim and Co-Propagating Crosstalk (FEXT) Calibration

Fig. 3-1 shows the block diagram for the Victim and Co-Propagating Crosstalk (FEXT) Calibration. The MCB and HCB are connected directly and not only is the victim signal calibrated, but also the FEXT (Far End Crosstalk) aggressor and NEXT (Near End Crosstalk) aggressor signals are calibrated too.
In this step, calibration of the Counter-Propagating (NEXT) Output Aggressors is performed and, as described later in Step 1-2: Counter-Propagating (NEXT) Calibration, the HCB and MCB connections are reconFig.d and the Counter-Propagating (NEXT) Input Aggressors Calibration is performed.
The bitrate of the PPG for the Counter Propagating Crosstalk (NEXT) calibration must be set to 14G.

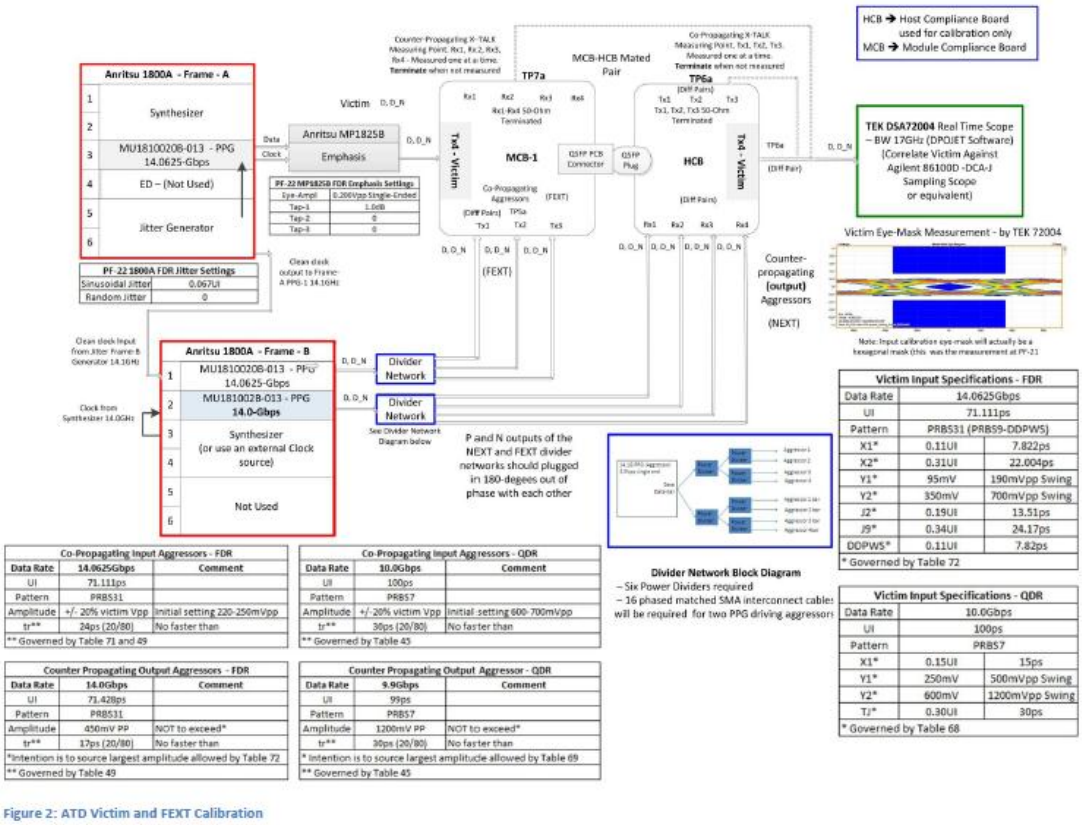


Figure 2: ATD Victim and FEXT Calibration

Fig. 3-1 Victim and Co-Propagating Crosstalk (FEXT) Calibration Block Diagram

Notice) For latest measurement method of compliance test, refer to the Active Cable Time-Domain Testing MOI provided by IBTA.

(1) Cabling and connecting victim signal (See Fig.3-2)

a. Connect a 30-cm cable (J1349A) from Clock Output of the internal Synthesizer (MU181000A/B) to External Clock Input of the Jitter Modulation Source (MU181500B).
b. When MU181000B without option-001 is used; Connect a 30-cm cable (J1349A) from Clock Output of the internal Synthesizer (MU181000A) to Aux Input of the Jitter Modulation Source (MU181500B).
   When MU181000A without option-001 is used; Split the Clock Output of the internal Synthesizer (MU181000A) and connect a 30-cm cable (J1349A) to Aux Input of the Jitter Modulation Source (MU181500B).
   When MU181000A/B with option-001 is used; connect a 30-cm cable (J1349A) from Trigger Output of the internal Synthesizer (MU181000A/B) to Aux Input of the Jitter Modulation Source (MU181500B).
c. Connect a 30-cm cable (J1349A) from Jittered Clock Output of the Jitter Modulation Source (MU181500B) to External Clock Input of the 14G PPG (MU181020B of MP1800A_Frame_B).
d. Connect two phase-matched cables from the victim PPG to the Emphasis Box (MP1825B). Connect one of these cables from Data Output of the PPG (MU181020B) to Data Input of the Emphasis Box (MP1825B). Connect the other cable from Clock Output of the PPG (MU181020B) to the Emphasis Box (MP1825B) Clock Input.
e. Connect two phase-matched cables from Data Output of the Emphasis Box (MP1825B) to the Tx4-Victim Input of the MCB.

(2) Cabling and connecting seven aggressor signals (See Fig.3-2)

a. Connect a cable from Reference Clock Output (select 1/1 to make the clock output 14.0625 Gbps) from the Jitter Modulation Source (MU181500B) to External Clock Input of the FEXT Aggressor PPG (MU181020B in slot_1 of MP1800A_Frame_A).
b. Connect one Clock Output from the Synthesizer (MU181000A/B of MP1800A_Frame_A via the P0047A Frequency Doubler and Z1340A BPF) to External Clock Input of the NEXT aggressor PPG (MU181020B in slot_2 of MP1800A_Frame_A). Note that another external synthesizer can be used instead of using the MU181000A/B Synthesizer, P0047 Frequency Doubler and Z1340A BPF.
c. Connect two PPG Data and XData signals to the Divider Network to generate 8 aggressor signals. (The eighth output is not used.)
d. Connect all seven aggressor signals to the evaluation board using 7 pairs of phase-matched cables. One of the eight outputs from the Divider Network is not used and should be terminated with 50Ω SMA terminators (on both Data and XData).

See Fig. 3-1 for other connections.

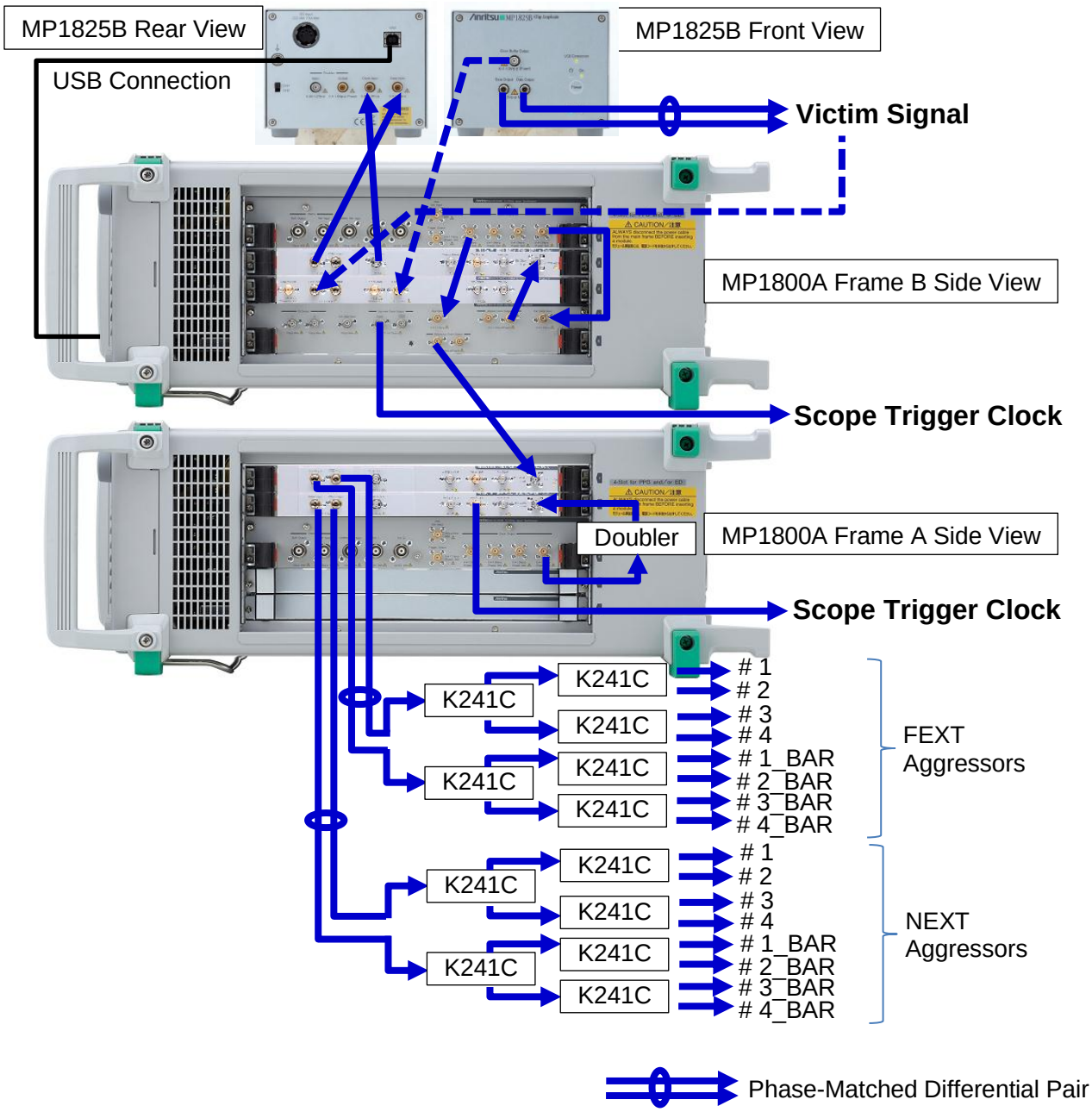


Fig. 3-2 Cabling of MP1800A, MP1825B and Divider Network

(3) Initial Setting of Victim Signal

a. Turn ON the MP1800A and select Main Application (automatically selected after 20 seconds). Open [File] at the top left of the MP1800A screen and select [Initialize].

b. Jitter Modulator Source Setting

- Select the number (6) at the Slot Keys of the MP1800A_Frame_B where the Jitter Modulator Source is installed.
- Select Internal Synthesizer (MU181000A/B) for the master clock.
- Set Clock Frequency to be 14.0625GHz.
- Select Pattern Generator Full-rate (MUX) for the jitter clock output.
- Check that all jitter settings are zero.
- Set the Sub-rate Clock output to 1/8 (1.7578125 GHz).

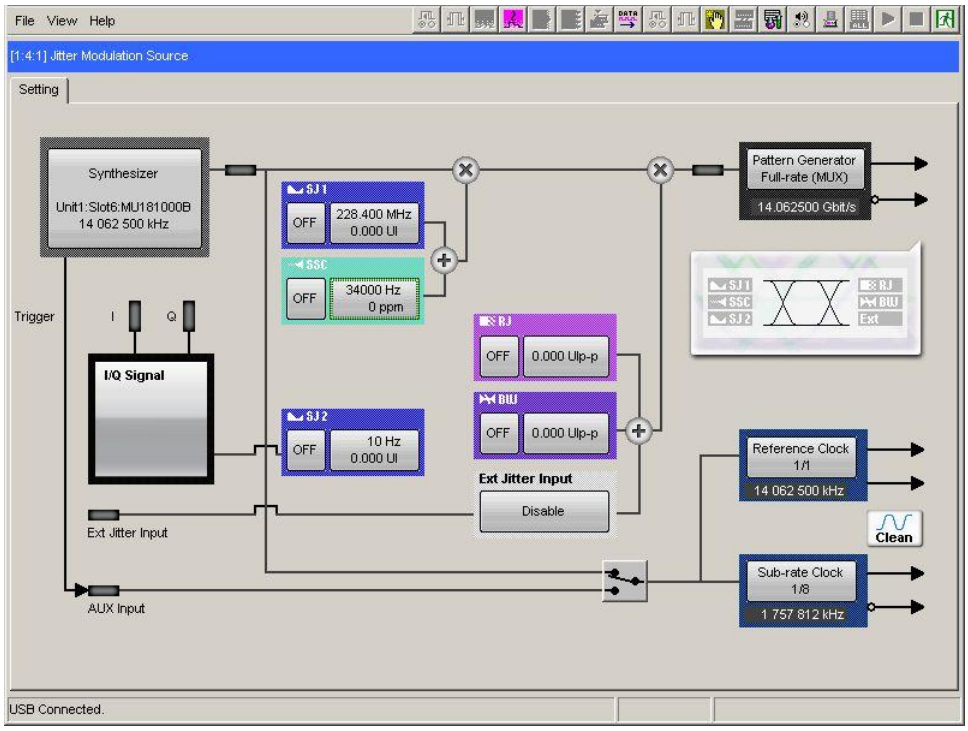


Fig. 3-3 MU181500B Jitter Modulation Source GUI

c. PPG Setting

- Select the number (3) from the Slot Keys of the MP1800A_Frame_B where the PPG is installed.
- Set the Data Output Amplitude to 500 mV (0.500 Vpp).
- Set the Offset (Vth) to Zero (0.000 V).
- Set the data pattern to PRBS 2^{31}-1.
- Press [OUTPUT ON] at the MP1800A front panel
- Set the AUX Output frequency division ratio on the Misc tab to 1/2.

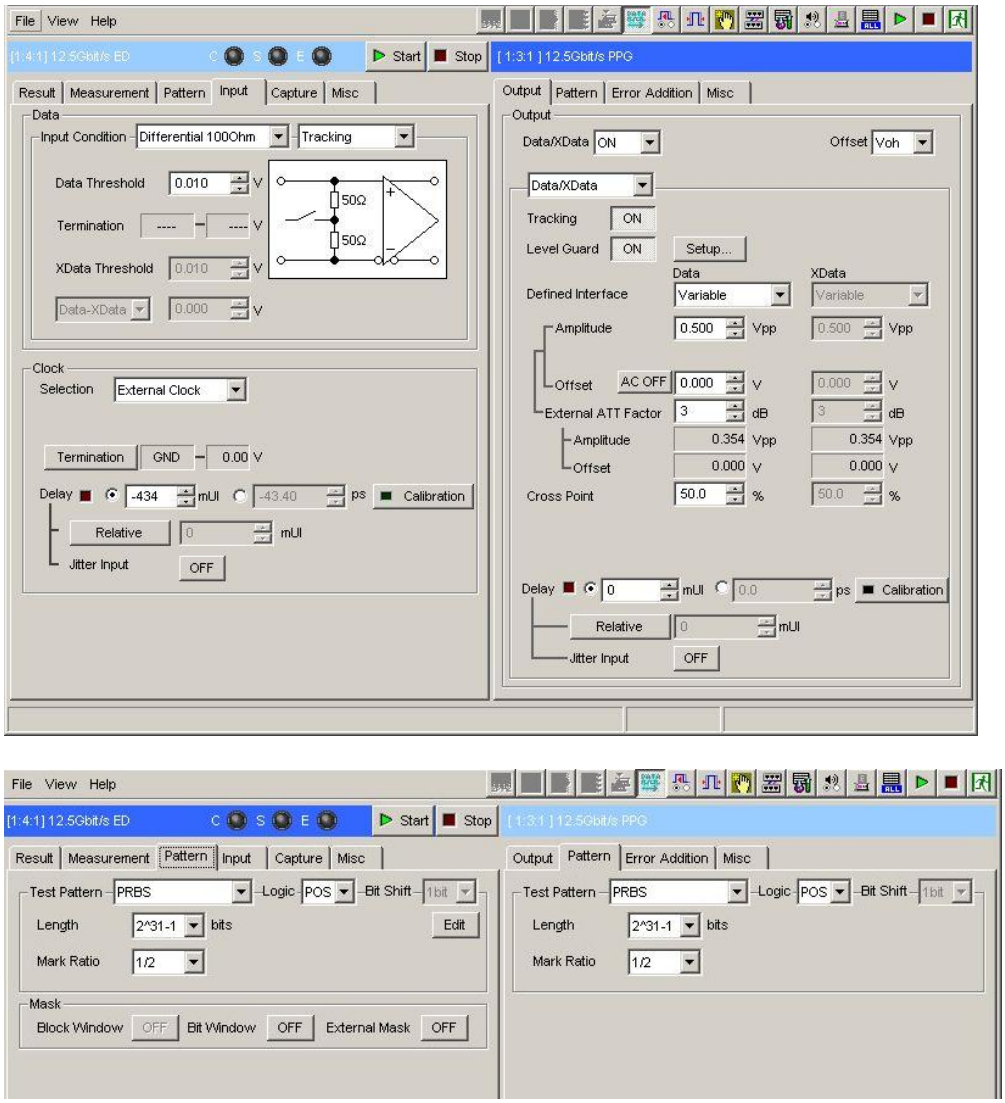


Fig. 3-4 MU181020B PPG GUI

d. Emphasis setting

- Turn ON the MP1825B power.
- Connect a USB cable from the MP1825B to one of the USB ports of the MP1800A_Frame_B. There are two USB ports on the front panel and one on the rear.
- Select the MP1825B icon at the top of the MP1800A screen.
- Select Connect at the MP1800A GUI to connect the MP1825B to the MP1800A.
- When clock doubler of MP1825B is used, press [Auto Adjust] to adjust skew between the incoming Data and Clock. This function can be used when clock doubler of MP1825B is used. When the phase matched cable are used as shown in Fig.3-2, Auto Adjust is not required.
- Set Eye Amplitude to 400 mV.
- Set Emphasis Function to OFF.
- Set Waveform Format to 1Post/1Pre-cursor
- Set Emphasis Output to ON.

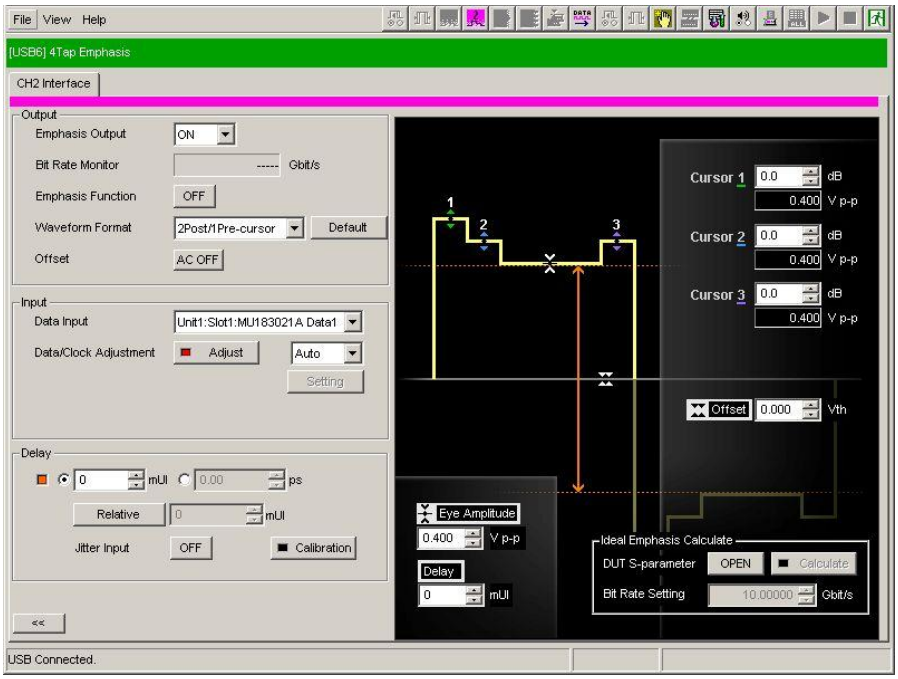


Fig. 3-5 MP1825B Emphasis Converter GUI

(4) Checking error free at looped-back connection (Optional)

Make a loopback connection from the PPG via the Emphasis Box to the Error Detector and check that no errors are detected to ensure the system is working correctly.

a. Connect three cables from the Emphasis Box (MP1825B) to the Error Detector (MU181040B).
   - Connect one pair of phase-matched cables from Output (Data and XData) of the Emphasis Box (MP1825B) to Data and XData Input of the Error Detector (MU181840B).
   - Connect the third cable from Clock Buffer Output of the Emphasis Box (MP1825B) to Clock Input of the Error Detector (MU181040B).

b. Error Detector Setting
   - Check that the green light of Data Output on the MP1800A_Frame_B front panel is ON. If it is OFF, press the Data Output key.
   - Select the number (4) from the Slot Keys of the MP1800A where the Error Detector is installed.
   - Set the input to Differential 100Ω.
   - Set the data pattern to PRBS 2^{31}-1.
   - Select the Auto Adjust Icon at the top of the MP1800A screen and put a checkmark in the Error Detector box (Auto Adjust ON)
   - Confirm that the Error Detector detects no errors (no red lights). See troubleshooting (Appendix) when NOT error-free.

c. Disconnect the phase-matched cables from the Error Detector (Data and XData) and connect them to the MCB Tx4-Victim Input.

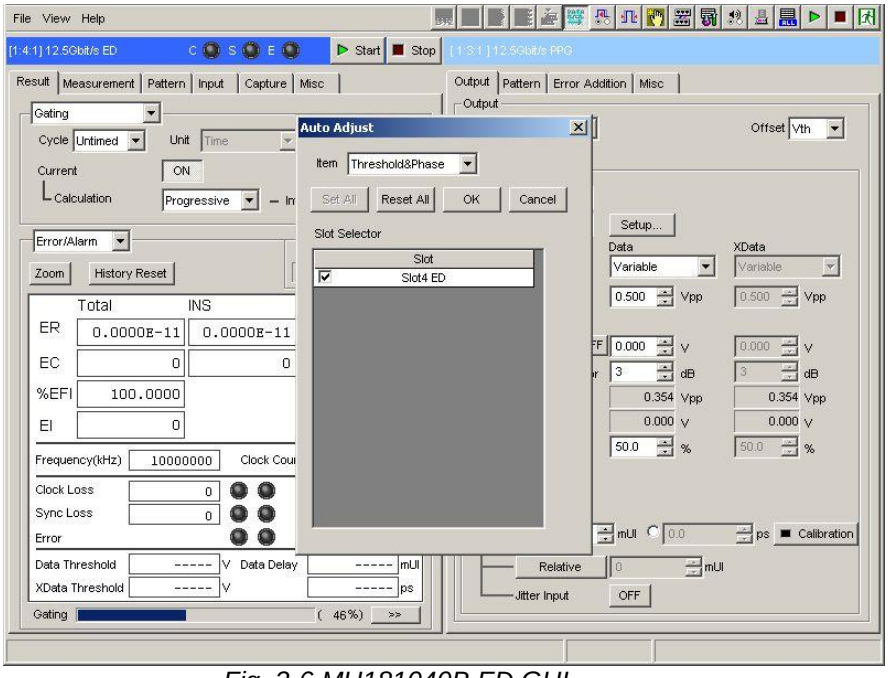


Fig. 3-6 MU181040B ED GUI

(5) Setting for Co-Propagating Input Aggressors (FEXT)

a. Connect a pair of phase-matched cables from the HCB TP6a differential output to the oscilloscope (Fig. 3-1).
b. Connect a cable from the Sub-rate Clock Output of the Jitter Modulation Source (MU181500B of the MP1800A_Frame_B) to the oscilloscope trigger input.
c. Turn ON the MP1800A_Frame_A of the aggressor signal and select Main Application (selected automatically after 20 seconds). Open [File] at the top left of the MP1800A screen and select [Initialize].
d. Initial setting of Aggressors
   - Select the number (1) from the Slot Keys of the MP1800A_Frame_A where the PPG is installed.
   - Set the Data and XData output amplitude to 1.0 V.
   - Set the Offset (Vth) to Zero.
   - Set the data pattern to PRBS 2^{31}-1.
   - Press OUTPUT ON at the MP1800A front panel .
e. Measure the differential eye amplitude of one of the aggressor signals at the HCB TP6a output using an oscilloscope.
f. Adjust the PPG amplitude so the HCB TP6a output is 220 - 250 mVpp (110 - 125 mV single-end) or less.
g. Terminate the HCB TP6a output connectors (both Data and XData) using 50Ω SMA terminators when the signals are not measured.

(6) Setting for Counter-Propagating Output Aggressors (NEXT)

a. Connect a pair of phase-matched cables from the MCB TP7a differential output to the oscilloscope (Fig. 3-1).
b. Connect a cable from the Aux output of the PPG (MU181020B of MP1800A_Frame_A) to the oscilloscope trigger clock input.
c. Synthesizer Setting
   - Select the number (4) from the Slot Keys of the MP1800A_Frame_A where the Synthesizer is installed.
   - Set Clock Frequency to 7.000 GHz. This clock is doubled to 14.0 GHz by the P0047A Frequency Doubler. Note that another external synthesizer can be used instead of using the MU181000A/B Synthesizer, P0047 Frequency Doubler, and Z1340A BPF.
d. Initial setting of Aggressors
   - Select the number (2) from the Slot Keys of the MP1800A_Frame_A where the PPG is installed.
   - Set the Data and XData output amplitude to 1.8 V.
   - Set the Offset (Vth) to Zero.
   - Set the data pattern to PRBS 2^{31}-1.
   - Press OUTPUT ON at the MP1800A front panel
   - Set the AUX Output frequency division ratio at the Misc tab to 1/8.
e. Measure the differential Eye amplitude of one of the aggressor signal at the MCB TP7a output using an oscilloscope.
f. Adjust the PPG amplitude so the MCB TP7a output is 450 mVpp (225 mV single end) or less.
g. Terminate the MCB TP7a output connectors (both Data and XData) using 50Ω SMA terminators when the signals are not measured.

(7) Victim Signal Calibration

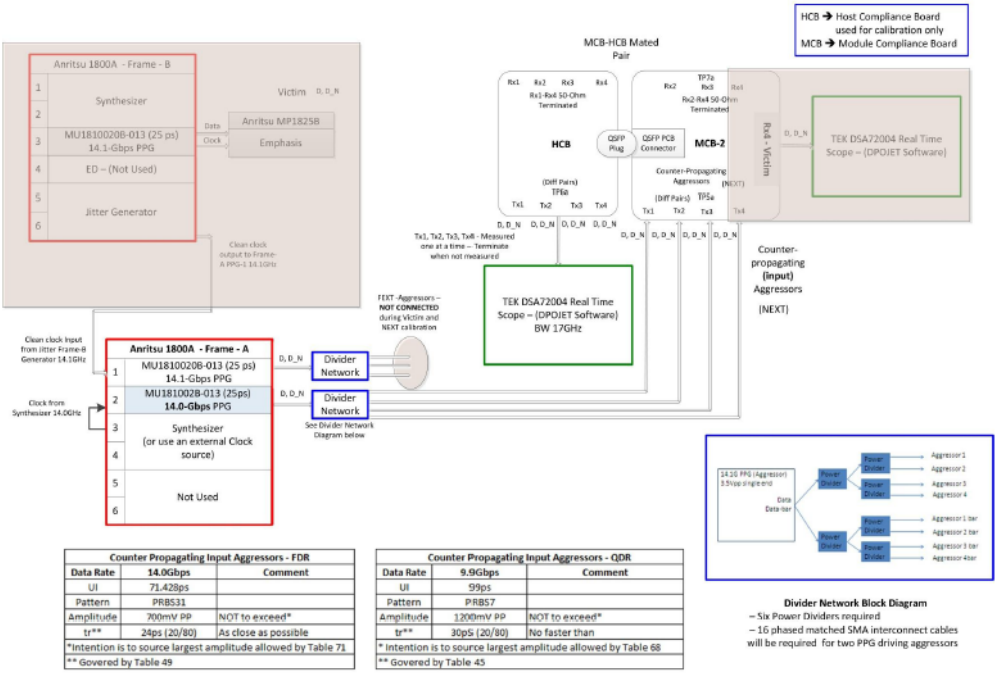
a. Connect a pair of phase-matched cables from TP6a TX4-Victim of the MCB to Scope (Fig. 3-1).
b. Connect a cable from Sub-rate Clock Output of the Jitter Modulation Source (MU181500B of MP1800A) to the oscilloscope trigger clock input.
c. Set the PPG (MU181020B) data pattern to PRBS 2^9-1.
d. Set the MP1825B Emphasis Function to ON.
e. Set all emphasis settings to zero.
f. Measure the data DDPWS (without jitter injection) using the oscilloscope to confirm it is within specification (0.11UI max. for InfiniBand FDR).
g. If the DDPWS is larger than the target specification, increase the amplitude of the first post-cursor emphasis until the DDPWS decreases to be within range. Add the pre-cursor amplitude when needed. Some trial and error may be required to find the best emphasis setting.
h. Set the PPG (MU181020B) data pattern to PRBS 2^{31}-1.
i. Measure J2/J9 using an oscilloscope and bathtub jitter.
j. Find the difference between the target J2 and J2 measured using the oscilloscope (MP2100A).
k. Set SJ1 of the Jitter Modulation Source (MU181500B) to ON.
l. Set the frequency of SJ1 of the Jitter Modulation Source (MU181500B) to 100 MHz.
m. Set the jitter amplitude of SJ1 to the difference calculated in step j.
n. Measure J2 again using the oscilloscope and adjust SJ1 so J2 is in the specified range (0.19 UI for InfiniBand FDR).
o. Measure J9 using an oscilloscope and find the difference between the target J9 and J9 measured by the oscilloscope.
p. Turn RJ of the Jitter Modulation Source (MU181500B) to ON.
q. Select None as the RJ filter.
r. Set the RJ amplitude to the difference calculated in step o.
s. Measure J9 again using the oscilloscope and adjust RJ of the Jitter Modulation Source so J9 is in the specific range (0.34 UI for InfiniBand FDR).
t. Adjust the Data amplitude of the Emphasis Box (MP1825B). The target waveform is shown in Fig. 3-1. (Y1 amplitude is the 190-mVpp differential).
u. Measure J2 and J9 again, and adjust SJ1 and RJ.
v. Check J2/J9, DDPWS and the output Eye (differential) and perform the Eye Mask test using the oscilloscope.

Table 3-4 Victim Input Specifications

Data Rate	14.0625 Gbps	
UI	71.111 ps	
Pattern	PRBS31	
X1	0.11 UI	7.822 ps
X2	0.31 UI	22.004 ps
Y1	95 mV	190 mVpp Swing
Y2	350 mV	700 mVpp Swing
J2	0.19 UI	13.511ps
J9	0.34 UI	24.177ps
DDPWS (PRBS9)	0.11UI(or less)	7.822ps (or less)

Step 1-2: Counter-Propagating (NEXT) Calibration

Switch the HCB and MCB connections and perform the Counter-Propagating (NEXT) Input Aggressors Calibration. Fig. 3-7 shows the block diagram at Counter-Propagating (NEXT) Calibration.



Counter Propagating Input Aggressors - FDR		
Data Rate	14.0Gbps	Comment
UI	71.428ps	
Pattern	PRBS31	
Amplitude	700mV PP	NOT to exceed*
tr**	24ps (20/80)	As close as possible
*Intention is to source largest amplitude allowed by Table 71		
** Govered by Table 49		

Counter Propagating Input Aggressors - QDR		
Data Rate	9.9Gbps	Comment
UI	99ps	
Pattern	PRBS7	
Amplitude	1200mV PP	NOT to exceed*
tr**	30pS (20/80)	No faster than
* Intention is to source largest amplitude allowed by Table 68		
** Govered by Table 45		

Figure 3: NEXT Calibration Diagram

Fig. 3-7 Counter-Propagating (NEXT) Calibration Block Diagram

Notice) For latest measurement method of compliance test, refer to the Active Cable Time-Domain Testing MOI provided by IBTA.

(1) Setting for Counter-Propagating Input Aggressors

a. Connect a pair of phase-matched cables from the HCB TP6a differential output to the oscilloscope (see Fig. 3-7 for other connections).
b. Connect a cable from Aux output of the PPG (MU181020B of MP1800A_Frame_A slot2) to the oscilloscope trigger clock input.
c. Synthesizer Setting (This is the same as Step1-1(6).)
   - Select the number (4) from the Slot Keys of the MP1800A_Frame_A where the Synthesizer is installed.
   - Set Clock Frequency to 7.000 GHz. This clock is doubled to 14.0 GHz by the P0047A Frequency Doubler. Note that another external synthesizer can be used instead of using the MU181000A/B Synthesizer, P0047 Frequency Doubler, and Z1340A BPF.
d. Initial setting of Aggressors (This is the same as Step1-1(6).)
   - Select the number (2) from the Slot Keys of the MP1800A_Frame_A where the PPG is installed.
   - Set Data and XData output amplitude to 3.5 V.
   - Set the Offset (Vth) to be Zero.
   - Set the data pattern to PRBS 2^{31}-1
   - Press OUTPUT ON at the MP1800A front panel.
   - Set the AUX Output frequency dividing ratio to 1/8 on the Misc tab
e. Measure the differential eye amplitude of one of the aggressor signals at the HCB TP6a output using the oscilloscope.
f. Adjust the PPG amplitude so the HCB TP6a output is 700 mVpp (350 mV single end) or less.
g. Terminate the HCB TP6a output connectors (both Data and XData) using 50Ω SMA terminators when the signals are not measured.

■ Step 2: Output Measurement

Connect the DUT between the two MCBs used at the Calibration Step and perform AOC evaluation. Fig. 3-8 shows the block diagram at DUT measurement.

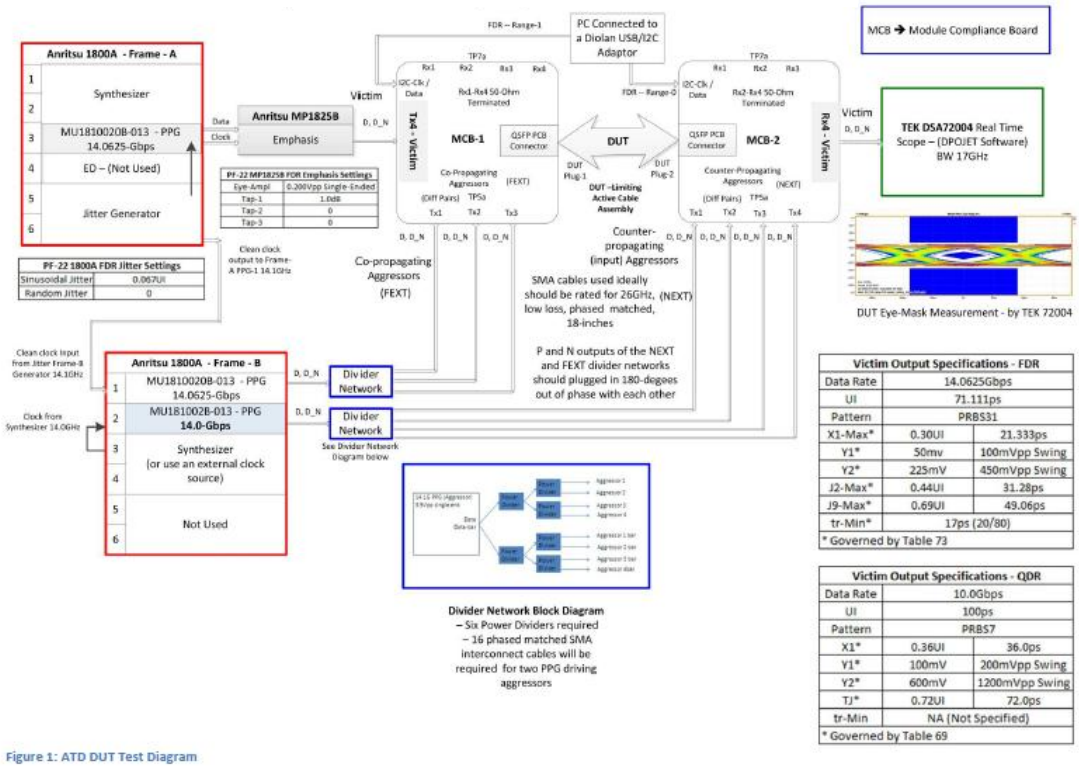


Fig. 3-8 DUT Testing – Output Measurement Block Diagram

Notice) For latest measurement method of compliance test, refer to the Active Cable Time-Domain Testing MOI provided by IBTA.

(1) Connect the DUT.
(2) Connect a pair of phase-matched cables from the MCB-2 TP7a RX4-Victim connector to the oscilloscope (see Fig. 3-8 for other connections).
(3) Set the parameters determined by the Step 1-1 Calibration for the Victim PPG (MP1800A_Frame_B) and Emphasis Box (MP1825B) and set output to ON.
(4) Set the parameters determined by the Step 1-1 Calibration for the Co-propagating Aggressor PPG (MU181020B in slot 1 of MP1800A_Frame_A) and set output to ON.
(5) Set the parameters determined by the Step 1-2 Calibration for the Counter-propagating Aggressor PPG (MU181020B in slot 2 of MP1800A_Frame_A) and set output to ON.
(6) Measure the output Eye (differential) using an oscilloscope. Perform the Eye Mask and jitter tests.

4. Conclusion

This article explains the method for evaluating 56G-IB-FDR QSFP+ AOC cables in the latest InfiniBand specifications. Achieving stable 4-channel duplex communications requires evaluation taking crosstalk between each channel. In addition, the measuring instruments required for stress-signal generation include a high-accuracy SJ and RJ modulator, a low-jitter and low-distortion PPG, and an emphasis converter for adjusting DDPWS at will.
The MP1800A Signal Quality Analyzer model lineup includes a PPG, ED, jitter modulation source, and emphasis converter supporting the high-accuracy measurement requirements for serial communications specifications, including InfiniBand and CEI.

Appendix

Troubleshooting if NOT error-free

(1) Check that the MP1800A Output is ON (green light on front panel). Check that the Emphasis output and PPG output are both set to ON.
(2) Check the PPG and ED patterns. (The PRBS pattern should be the same.)
(3) Check that the ED Auto Adjust function is ON.
(4) Check the length of the paired phase-matched cables. (Try single-end cables.)
(5) Check that the ED clock is 14.0625G. If the clock is not 14.0625G, check the cable connection.

References

[1] InfiniBand Architecture Specification Volume2 Release 1.3, IBTA, 2012/Nov/6
[2] Jitter Analysis - Basic Classification of Jitter Components using Sampling Scope,
Anritsu Corporation, Application Note No. MP2100A-E-F-3
[3] Signal Integrity Analysis of 28 Gbit/s High-Speed Digital Signal,
Anritsu Corporation, Application Note No. MP1800A-Signal_Integrity-E-F-1

Anritsu

Specifications are subject to change without notice.

● **United States**
Anritsu Company
1155 East Collins Blvd., Suite 100, Richardson,
TX 75081, U.S.A.
Toll Free: 1-800-267-4878
Phone: +1-972-644-1777
Fax: +1-972-671-1877

● **Canada**
Anritsu Electronics Ltd.
700 Silver Seven Road, Suite 120, Kanata,
Ontario K2V 1C3, Canada
Phone: +1-613-591-2003
Fax: +1-613-591-1006

● **Brazil**
Anritsu Eletrônica Ltda.
Praça Amadeu Amaral, 27 - 1 Andar
01327-010 - Bela Vista - São Paulo - SP - Brazil
Phone: +55-11-3283-2511
Fax: +55-11-3288-6940

● **Mexico**
Anritsu Company, S.A. de C.V.
Av. Ejército Nacional No. 579 Piso 9, Col. Granada
11520 México, D.F., México
Phone: +52-55-1101-2370
Fax: +52-55-5254-3147

● **United Kingdom**
Anritsu EMEA Ltd.
200 Capability Green, Luton, Bedfordshire, LU1 3LU, U.K.
Phone: +44-1582-433200
Fax: +44-1582-731303

● **France**
Anritsu S.A.
12 avenue du Québec, Bâtiment Iris 1- Silic 612,
91140 VILLEBON SUR YVETTE, France
Phone: +33-1-60-92-15-50
Fax: +33-1-64-46-10-65

● **Germany**
Anritsu GmbH
Nemetschek Haus, Konrad-Zuse-Platz 1
81829 München, Germany
Phone: +49-89-442308-0
Fax: +49-89-442308-55

● **Italy**
Anritsu S.r.l.
Via Elio Vittorini 129, 00144 Roma, Italy
Phone: +39-6-509-9711
Fax: +39-6-502-2425

● **Sweden**
Anritsu AB
Borgarfjordsgatan 13A, 164 40 KISTA, Sweden
Phone: +46-8-534-707-00
Fax: +46-8-534-707-30

● **Finland**
Anritsu AB
Teknobulevardi 3-5, FI-01530 VANTAA, Finland
Phone: +358-20-741-8100
Fax: +358-20-741-8111

● **Denmark**
Anritsu A/S (Service Assurance)
Anritsu AB (Test & Measurement)
Kay Fiskers Plads 9, 2300 Copenhagen S, Denmark
Phone: +45-7211-2200
Fax: +45-7211-2210

● **Russia**
Anritsu EMEA Ltd.
Representation Office in Russia
Tverskaya str. 16/2, bld. 1, 7th floor.
Russia, 125009, Moscow
Phone: +7-495-363-1694
Fax: +7-495-935-8962

● **United Arab Emirates**
Anritsu EMEA Ltd.
Dubai Liaison Office
P O Box 500413 - Dubai Internet City
Al Thuraya Building, Tower 1, Suit 701, 7th Floor
Dubai, United Arab Emirates
Phone: +971-4-3670352
Fax: +971-4-3688460

● **India**
Anritsu India Private Limited
2nd & 3rd Floor, #837/1, Binnamangla 1st Stage,
Indiranagar, 100ft Road, Bangalore - 560038, India
Phone: +91-80-4058-1300
Fax: +91-80-4058-1301

● **Singapore**
Anritsu Pte. Ltd.
60 Alexandra Terrace, #02-08, The Comtech (Lobby A)
Singapore 118502
Phone: +65-6282-2400
Fax: +65-6282-2533

● **P.R. China (Shanghai)**
Anritsu (China) Co., Ltd.
Room 2701-2705, Tower A,
New Caohejing International Business Center
No. 391 Gui Ping Road Shanghai, 200233, P.R. China
Phone: +86-21-6237-0898
Fax: +86-21-6237-0899

● **P.R. China (Hong Kong)**
Anritsu Company Ltd.
Unit 1006-7, 10/F., Greenfield Tower, Concordia Plaza,
No. 1 Science Museum Road, Tsim Sha Tsui East,
Kowloon, Hong Kong, P.R. China
Phone: +852-2301-4980
Fax: +852-2301-3545

● **Japan**
Anritsu Corporation
8-5, Tamura-cho, Atsugi-shi, Kanagawa, 243-0016 Japan
Phone: +81-46-296-1221
Fax: +81-46-296-1238

● **Korea**
Anritsu Corporation, Ltd.
502, 5FL H-Square N B/D, 681
Sampyeong-dong, Bundang-gu, Seongnam-si,
Gyeonggi-do, 463-400 Korea
Phone: +82-31-696-7750
Fax: +82-31-696-7751

● **Australia**
Anritsu Pty. Ltd.
Unit 21/270 Ferntree Gully Road, Notting Hill,
Victoria 3168, Australia
Phone: +61-3-9558-8177
Fax: +61-3-9558-8255

● **Taiwan**
Anritsu Company Inc.
7F, No. 316, Sec. 1, NeiHu Rd., Taipei 114, Taiwan
Phone: +886-2-8751-1816
Fax: +886-2-8751-1817

1306

Please Contact:

Printed on Recycled Paper

No. MP1800A_IBFDR_AOC-E-F-1-(1.00) Printed in Japan 2013-7 MG